CLAIMS

I claim:

1. A system for determining criticality in an electrical circuit comprising:
    a. a netlist input for receiving a circuit netlist, the netlist representing a topology of the electrical circuit;
    b. an assertion input for receiving one or more assertions representing boundary timing conditions;
    c. a delay variability input for receiving a list of one or more sources of delay variation that contain variability information of one or more of the sources of delay variation;
    d. a model input for receiving a parameterized delay model, the parameterized delay model containing a model for the delay of each component of the electrical circuit, each model being a function of one or more of the sources of variation; and
    e. a process that determines and outputs timing criticality information of the electrical circuit.

2. A system, as in claim 1, where the timing criticality information is a node criticality probability of one or more nodes of the electrical circuit.

3. A system, as in claim 1, where the timing criticality information is a component criticality probability of one or more components of the electrical circuit.

4. A system, as in claim 1, where the timing criticality information is the criticality probability of one or more paths of the electrical circuit.

5. A system, as in claim 4, where the criticality probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

6. A system, as in claim 4, where the criticality probability of a node of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that node.

7. A system, as in claim 4, where the arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

8. A system, as in claim 4, where the required arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

9. A system, as in claim 1, where the timing criticality information is used to determine a path through the circuit that has the highest probability of being critical.

10. A system, as in claim 1, where the timing criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

11. A system, as in claim 1, where the timing criticality information is used to determine one or more critical paths in order of criticality probability until the sum of the criticality probabilities exceeds a user-provided probability threshold.

12. A method, as in claim 1, where the timing criticality information is determined on the basis of the overall electrical circuit.

13. A method, as in claim 1, where the timing criticality information is determined on the basis of a single end point.

14. A system, as in claim 1, where a late-mode criticality information is determined from the timing criticality information.

15. A system, as in claim 1, where an early-mode criticality information is determined from the timing criticality information.

16. A system, as in claim 1, where a separate rising and a separate falling criticality information is determined from the timing criticality information for each of the one or more nodes of the electrical circuit and for each of the one or more components of the electrical circuit.

17. A system, as in claim 1, where the electrical circuit is one or more of the following types: a combinational circuit, a sequential circuit, a static logic circuit, and a dynamic logic circuit.

18. A system, as in claim 1, where the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

19. A system, as in claim 18, where the guard time of each timing test is one of deterministic and statistical.

20. A system, as in claim 1, where the electrical circuit contains multiple clock phases.

21. A system, as in claim 1, where the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part,

a correlated part, and an independently random part.

22. A system, as in claim 21, where the sources of variation are correlated.

23. A system, as in claim 21, where the sources of variation are independent.

24. A system, as in claim 1, where the parameterized delay models are pre-stored in a table.

25. A system, as in claim 1, where the parameterized delay models are pre-stored as coefficients of delay equations.

26. A system, as in claim 1, where the parameterized delay models are determined by circuit simulation on-the-fly.

27. A system, as in claim 1, where each assertion is one of deterministic and statistical.

28. A system, as in claim 1, where clock-edge information is one of deterministic and statistical.

29. A method for determining criticality information of an electrical circuit, comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing the arrival tightness and required arrival tightness probabilities at each of the one or more edges of the electrical circuit; and

e. determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

30. A method for determining criticality information of an electrical circuit, comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of the one or more end points of the timing graph; and

f. determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

31. A method, as in claims 29 and 30, where the timing criticality information is the criticality probability of one or more paths of the electrical circuit.

32. A method, as in claims 29 and 30, where the criticality probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

33. A method, as in claims 29 and 30, where the criticality probability of a node of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that node.

34. A method, as in claims 29 and 30, where the arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

35. A method, as in claims 29 and 30, where the required arrival tightness probability of a component of the electrical circuit is used as an upper bound on the path criticality probability of any path of the electrical circuit including that component.

36. A method, as in claims 29 and 30, where the criticality information is used to determine the path that has the highest probability of being critical.

37. A method, as in claims 29 and 30, where the criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

38. A method, as in claims 29 and 30, where the criticality information is used to determine a user-provided number of critical paths in order of criticality probability.

39. A method, as in claims 29 and 30, where the criticality information is used to determine critical paths in order of criticality probability until the sum of the criticality probabilities exceeds a user-provided probability threshold.

40. A method, as in claim 30, where the criticality probabilities are determined on the basis of the overall electrical circuit.

41. A method, as in claim 29, where the criticality probabilities are determined on the basis of a single end point.

42. A method, as in claims 29 and 30, where late-mode criticality information is determined.

43. A method, as in claims 29 and 30, where early-mode criticality information is determined.

44. A method, as in claims 29 and 30, where separate rising and falling criticality information is determined for each of the one or more nodes of the timing graph and for each of the one or more edges of the timing graph.

45. A method, as in claims 29 and 30, where the electrical circuit is one or more of the following: a combinational circuit, a sequential circuit, a static logic circuit, and a dynamic logic circuit.

46. A method, as in claims 29 and 30, where the electrical circuit is a sequential circuit that contains one or more of the following: an edge-triggered latch, a master-slave latch, a level-sensitive latch, and a transparent latch.

47. A method, as in claims 29 and 30, where the guard time of each timing test is one of deterministic and statistical.

48. A method, as in claims 29 and 30, where the circuit contains multiple clock phases.

49. A method, as in claims 29 and 30, where the parameterized delay model for each component of the electrical circuit comprises one or more of: a deterministic part, a correlated part, and an independently random part.

50. A method, as in claims 29 and 30, where the sources of variation are correlated.

51. A method, as in claims 29 and 30, where the sources of variation are independent.

52. A method, as in claims 29 and 30, where the parameterized delay models are pre-stored in a table.

53. A method, as in claims 29 and 30, where the parameterized delay models are pre-stored as coefficients of delay equations.

54. A method, as in claims 29 and 30, where the parameterized delay models are determined by circuit simulation on-the-fly.

55. A method, as in claims 29 and 30, where each assertion is one of deterministic and statistical.

56. A method, as in claims 29 and 30, where clock-edge information is one of deterministic and statistical.

57. A system for determining criticality information of an electrical circuit, comprising:

a. means for reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for conducting a statistical timing analysis of the electrical circuit;

d. means for storing an arrival tightness and a required arrival tightness probability at each of the one or more edges of the electrical circuit; and

e. means for determining the criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

58. A system for determining criticality information of an electrical circuit, comprising:

a. means for reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. means for building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. means for conducting statistical timing analysis of the electrical circuit;

d. means for storing an arrival tightness and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. means for determining an end point criticality probability of each of the one or more end points of the timing graph; and

f. means for determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

59. A memory storage device storing a method for determining criticality information of an electrical circuit, the method comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing an arrival tightness and a required arrival tightness probabilities at each of the one or more edges of the electrical circuit; and

e. determining a criticality timing probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

60. A memory storage device storing a method for determining criticality information of an electrical circuit, the method comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of the one or more end points of the timing graph; and

f. determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.

61. An output product produced by a process for determining criticality information of an electrical circuit, the process comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting a statistical timing analysis of the electrical circuit;

d. storing an arrival tightness and a required arrival tightness probabilities at each of the one or more edges of the electrical circuit; and

e. determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal

of the timing graph.

62. An output product produced by a process for determining criticality information of an electrical circuit, the process comprising the steps of:

a. reading a netlist, one or more assertions, one or more parameterized delay models and a list of one or more sources of variation;

b. building a timing graph that represents the electrical circuit, the timing graph having one or more nodes and one or more edges;

c. conducting statistical timing analysis of the electrical circuit;

d. storing an arrival tightness and a required arrival tightness probability at each of the one or more edges of the electrical circuit;

e. determining an end point criticality probability of each of the one or more end points of the timing graph; and

f. determining a criticality probability of one or more nodes of the timing graph and one or more edges of the timing graph by a backward traversal of the timing graph.